REMARKS

It is submitted, for the reasons set forth below, that the claims should be allowed and the application passed to issue.

I. Rejections under 35 U.S.C. § 102(e)

Claims 1, 2, 6 -12, and 14 - 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent No. US 6492872 issued to Fujioka et al. (herein "Fujioka").

These rejections are traversed.

As to claim 1, the rejection under 35 U.S.C. § 102(e) of claim 1 as being anticipated by Fujioka is traversed on the grounds that Fujioka does not teach, suggest or render obvious all the limitations of claim 1.

For example, claim 1 recites, in part "A method for improving an input match in a circuit comprising: operating a **cascode** having ..." (emphasis added). The Examiner wrote *"... Regarding to claim 1, Fig. 9 Fujioka et al. disclose a method for improving an input match in a circuit comprising: operating a cascade having... "* (emphasis added).

It is respectfully submitted that Fujioka teaches *cascade* circuits but does not teach or disclose *cascode* circuits. Moreover, cascode circuits and cascade circuits are well-known to be distinct in the art and that it is not obvious to apply operating principles for cascades to cascodes. If the examiner wishes, an Engineering opinion from a Registered Electrical Engineer to this effect will be submitted in the form of an affidavit.

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Moreover, claim 1 recites, in part "...operating a cascode having an input signal port with an input signal impedance ... and operating an impedance compensating circuit for changing a compensating impedance presented at the input signal port, wherein the impedance compensating circuit is controlled by the level setting gain control voltage...". The Examiner wrote "... *Regarding to claim 1, Fig. 9 Fujioka et al. disclose ... operating a cascade having an input signal port (Gate of Q1) with an input signal impedance (MC1) ... and operating an impedance compensating circuit for changing a compensating impedance presented at the input signal port (22), wherein the impedance compensating circuit is controlled by the level setting gain control voltage (Vapc) and wherein the impedance compensating circuit is operable to counteract changes in the input signal impedance correlated with changes in the stage gain (Fig. 14, 15)...*".

It is respectfully submitted that in reference to Fujioka Fig. 9, Fujioka teaches that MC1 is a matching circuit rather than an input impedance (Fujioka Col. 10, line 53) and that matching circuits and input impedances circuits are well-known to be distinct in the art. It is further respectfully submitted that the examiner has not shown where Fujioka teaches or discloses an impedance compensation circuit; indeed Fujioka is entirely silent as to compensation circuits. It is further respectfully submitted that the examiner has not shown where Fujioka teaches or discloses where an impedance of controlled by Vapc, let alone a compensating impedance as recited in claim 1.

Thus, for at least the reasons stated above a prima facie case for anticipation of claim 1 has not been made and allowance of claim 1 under 35 U.S.C. § 103(e) is respectfully requested.

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As regards Claims 2, 6 and 7, they are dependent on claim 1 and so are allowable for at least the same reasons as claim 1, therefore allowance of claims 2, 6 and 7 is respectfully requested.

As to claims 8 and 16, the rejection under 35 U.S.C. § 102(e) of claims 8 and 16 as being anticipated by Fujioka is traversed on the grounds that Fujioka does not teach, suggest or render obvious all the limitations of claim 8 nor of claim 16.

Again the examiner is impermissibly citing cascade circuits as prior art for cascode circuits and mischaracterizing circuit blocks. For example, the examiner wrote "...*Regarding to claims 8, and 16, Fig. 11 Fujioka et al. disclose ... a gain controller (22) operable to adjust a gain of the cascade in response to a control signal (22);* ... ". But Fujioka identifies circuit 22 of Fig. 11 only as a gate bias circuit (GBC) (Col. 11, lines 55-58) and not as a gain controller nor as a control signal. Gate bias circuits, gain controllers and control signals are well-known to be distinct in the art.

Thus, for at least the reasons stated above a prima facie case for anticipation of claims 8 and 16 has not been made and allowance of claims 8 and 16 under 35 U.S.C. § 103(e) is respectfully requested.

As regards claims 9 – 14 and 15, they are dependent on claim 8 and so are allowable for at least the same reasons as claim 8, therefore allowance of claims 9 – 14 and 15 is respectfully requested.

As regards claims 17 - 19, they are dependent on claim 8 and so are allowable for at least the same reasons as claim 8, therefore allowance of claims 17 – 19 is respectfully requested.

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II. Rejections under 35 U.S.C. § 103(a)

Claims 3 – 5, 13 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over (sic, rendered obvious by) Fujioka.

It is respectfully submitted that claims 3 – 5 are dependent on claim 1, claim 13 is dependent on claim 8 and claim 20 is dependent on claim 16, therefore claims 3 – 5, 13 and 20 are allowable for at least the same reasons as claims 8, 16 and 20 respectively and allowance of claims 3 – 5, 13 and 20 is respectfully requested.

SUMMARY

Claims 1-20 are pending in this application. Claims 1-20 were rejected.

It is respectfully requested that the Examiner reconsider and allow the rejected claims for the reasons stated and pass this case to issue with all of pending claims 1-20 allowed.

The examiner is invited to call the undersigned at (650) 726 3901 if desired to help advance prosecution.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

_____, 2003.

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Agent Date of Signature

Respectfully submitted,

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